SAME 2006 Forum

Session 5 : CLOCK TECHNOLOGY

Analysis of Clock Jitter using PsiWinder

Bhavana Thudi (bthudi@apache-da.com)
Ying-Shiun Li (ying@apache-da.com)
Ichiang Lin (ilin@apache-da.com)

Apache Design Solutions, Inc.
Mountain View, CA, USA

Abstract:

In this paper, we present a tool PsiWinder that can analyze clock jitter in the presence of simultaneous power-grid and signal coupling noise. As we move to 90nm processes and below, with reducing power supply voltages and noise margins, the dynamic nature of power grid noise and its impact on timing must be considered. In addition, with higher operating frequencies and design complexities, signal cross-talk, simultaneous switching noise, and dynamic voltage drop must all be accounted for concurrently.

Introduction

Jitter is defined as the deviation of a timing event of a signal from its ideal position. Jitter sources can be both random and deterministic. Clock signals are typically susceptible to deterministic jitter which can be caused from noise sources such as crosstalk, simultaneous switching outputs, and dynamic power-grid noise.

Reduction in the power supply causes a reduction in the drive strength when a device needs power to make a transition. Such voltage fluctuations are localized and depend on among other things, the strength of the power distribution network, the logic gates and their drive strengths, and the resulting switching events in that region. The true transient nature of this power supply noise is not captured in existing timing solutions, which use an effective, ideal or constant Vdd/Vss approximation for instance supply voltages. Cross-coupling capacitance between neighbouring nets can aggravate the noise impacting both the delay and the functionality of the circuit. In the deep sub-micron regime, it is no longer acceptable to ignore these concurrent noise sources. A solution that addresses this problem must consider both signal and power supply noise concurrently, taking into account the true dynamic nature of the problem.

In the paper, we will describe the different causes of clock jitter and the need to analyze both signal and power supply noise together efficiently. We will then elaborate on the key technologies used for this analysis. Results will be presented showing the effect on clock jitter from different noise sources.

Power supply and signal noise impact on clock jitter

Advances in semiconductor manufacturing are enabling complex circuit designs with higher speeds and densities. This causes the on-chip power grid network to experience large dynamic voltage fluctuations. These power supply variations depend on the switching activity over time, on-chip RLC networks, L di/dt noise, LC resonance noise and off-chip package RLC. The analog variation in the power supply impacts the delay as shown in Figure 1.

Considering the effects of both signal and power noise simultaneously is critical for this analysis. Cross-coupling capacitance across clock nets and neighboring nets can cause a decrease or increase in the clock delay. If the coupled-nets are switching in the opposite direction, the delay will increase. If they are switching in the same direction, the delay will decrease. This noise component together with the power supply noise can cause an unpredictable variation in the clock delay or jitter. Figure 2 below shows these effects.

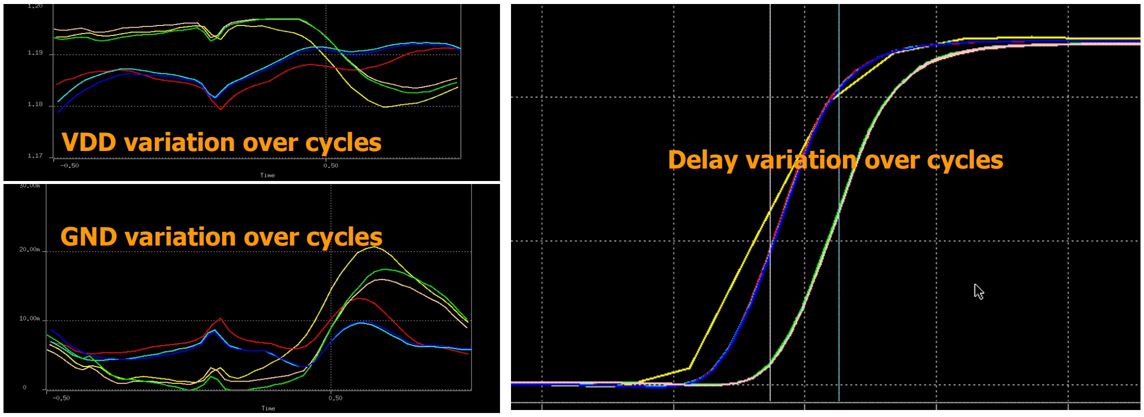

Figure 1 Impact of voltage drop on delay

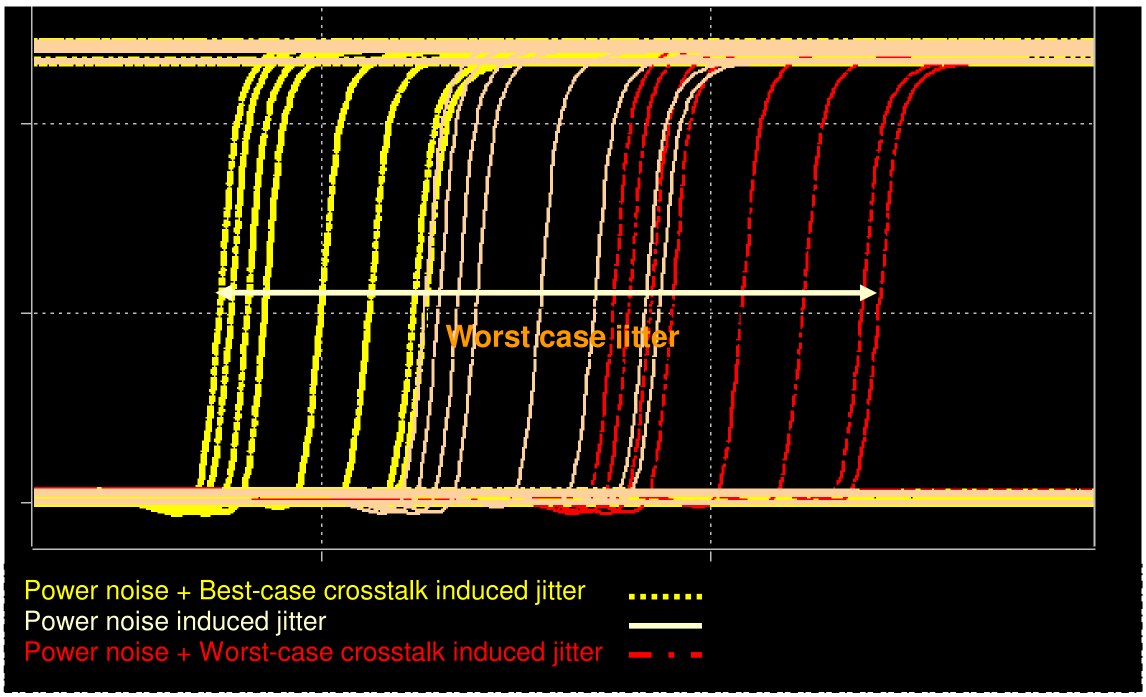

Figure 2 Power and signal noise impact on jitter

The worst case jitter in Figure 2 is measured as the maximum variation in the clock period. The worst case supply variation is first determined by the various on-chip and off-chip transient effects. In addition, the simultaneous impact of crosstalk noise can increase or decrease the clock delay.

PsiWinder key technologies and solutions

PsiWinder is a critical path and clock network timing sign-off solution for high-performance nanometer designs. It is a dynamic timing solution that utilizes a true-Spice simulator. It accurately considers the effects of dynamic voltage drop (DvD) and ground bounce on timing. This power noise is typically computed from a true transient analysis of the full-chip power grid considering simultaneous switching, package and decap effects. Commercially available Dynamic Voltage Drop analysis tools like RedHawk are capable of generating sign-off quality DvD waveforms for every instance in the design. PsiWinder utilizes the instance specific Vdd/Vss waveforms, which is not only a function of that cell's switching activity but is also dependent of all the neighboring cell's activity and quality of the power grid in the design. It combines the effect of DvD with signal coupling noise to accurately analyze the timing of the clock network.

Spice should be the golden sign-off for silicon accurate simulation. However, with the capacity and performance limitations of traditional Spice simulators, it is impossible to simulate an entire SOC design. It is time consuming and error prone for a designer to generate a Spice netlist that contains the clock tree including the coupling network, coupling drivers and receivers, and power / ground supply network. In addition, traditional Spice simulators are limited in their capacity and performance to simulate the clock tree.

PsiWinder delivers full-chip capacity with a Spice-accurate simulation of clock networks, including all the nanometer and high-speed effects such as crosstalk and DvD. PsiWinder utilizes a true Spice simulator with its proprietary BLSN (big linear, small non-linear) technology to accelerate the solving of networks that have an enormous number of linear elements, and a smaller number of non-linear elements.

PsiWinder automatically generates a Spice netlist containing all the devices in a clock tree including the parasitics in the routing, and potential aggressors coupled to the nodes in the path by applying instance-specific Vdd/Vss waveforms to all the power and ground pins of the gates in the clock tree, and is capable of running distributed Spice simulation using LSF and/or Sun Grid for higher throughput. It also utilizes a clustering algorithm for circuit partitioning to achieve highly efficient analysis.

Clock signals are susceptible to periodic jitter and duty cycle distortion (DCD). Periodic jitter is the change in the clock period and DCD is the variation in the duty cycle from cycle-to-cycle. We can capture these clock jitter effects with multi-cycle simulations using different switching scenarios sensitizing different logic and state conditions in each cycle. Measuring the clock period and duty cycle of each node of the clock tree network for every cycle enables us to measure the worst case jitter between consecutive clock cycles and among all simulation cycles.

Capturing the worst case jitter is dependent on generating the worst-case switching scenarios and event sequences for peak dynamic voltage drop. Generating vectors for this purpose can be very difficult and in most cases impossible. For this reason, it is important to compute the statistical worst-case switching scenarios and event sequences for peak dynamic voltage drop without requiring user-provided vectors. Exploring the physical design to highlight weaknesses which are more susceptible to voltage drop and in turn to clock jitter effects is also essential. This broadens the coverage to power/ground network structural weaknesses that is not covered in any existing timing analysis solution.

Designs with multiple frequency domains must be analyzed accurately to consider the interference of the different frequency domains. This is especially true when an instance from one frequency domain is injecting power supply noise to a neighboring clock net in a different frequency domain causing the switching in the two domains to align. Low power designs with some portions of the design powering up from the off-state with other blocks in an off state or on state can be subject to ramp-up noise. Clock gating designs must also be carefully analyzed when the gated cells are being turned on. Therefore, advanced design styles must be carefully analyzed in a transient simulation taking into account the different operating modes of the chip.

The worst case clock jitter is also dependent on the worst case signal cross-talk. The switching direction of neighbouring signals and cross-talk noise alignment is considered in PsiWinder along with the dynamic voltage drop for realistic analysis.

It is essential to analyze various on-chip and off-chip phenomena such as simultaneous switching noise of core, memory and I/O, intentional and intrinsic decoupling capacitance, on-chip inductance and package parasitics. Incorporating these complex effects in a noise analysis is critical to its accuracy.

Results

In this section, we present clock jitter analysis using PsiWinder on the clock network of a 90nm design. The example illustrates the different causes for clock jitter and how the jitter issue was fixed incorporating both on-chip and off-chip phenomenon in the analysis.

The chip supply current depends on the on-die and package decoupling capacitance and inductance. The decoupling capacitance behaves as a local reservoir of charge supplying current to switching instances in the region. Thus the chip’s total switching current profile and supply current profile can be very different. In Figure 3 the difference in the current profiles is the current supplied by the decoupling capacitors. Even though the switching current profile of a clock node can be repetitive every cycle, the supply current and thus the supply volatge varies over the different cycles because of the significant capacitive and inductive components. For this reason including the package C and L is important for the simulation.

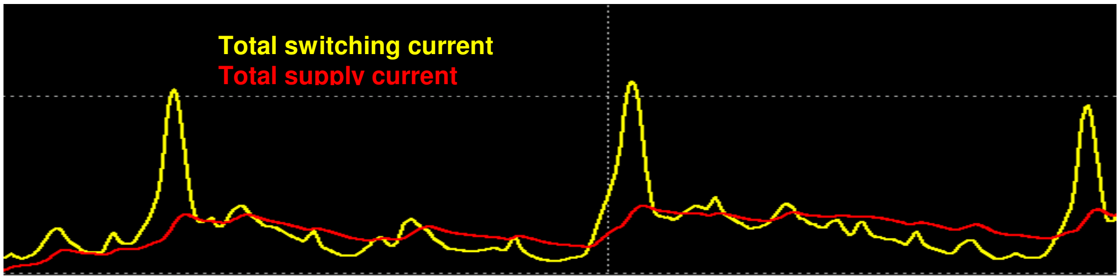

Figure 3 Chip current profile

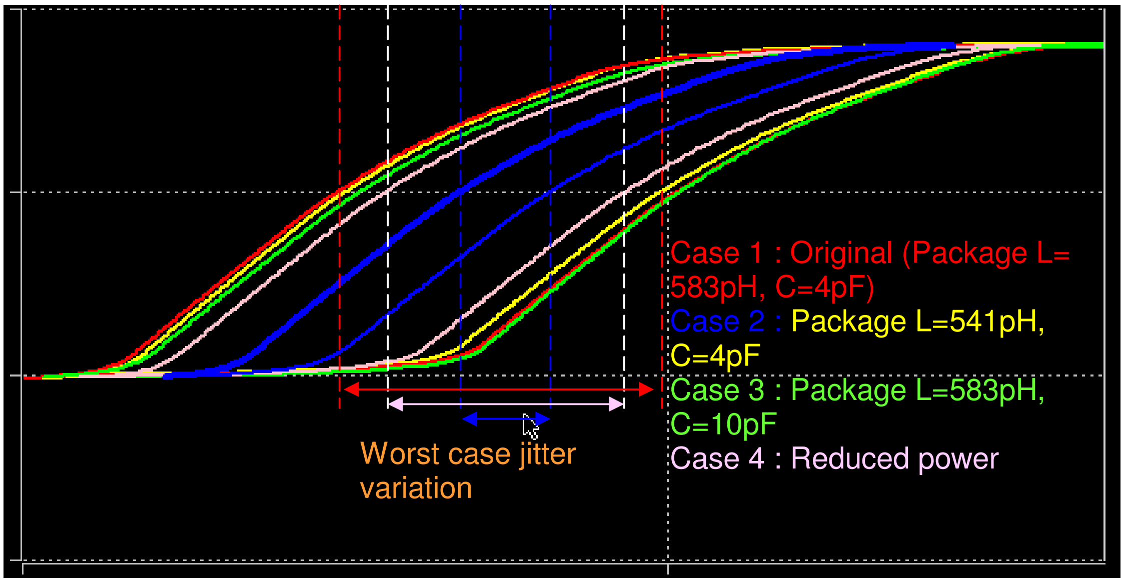

Figure 4 Worst case jitter variations

In this example, the clock period was measured over eight cycles where the power/ground supply voltage waveform varies over the cycles. The worst case jitter, defined as the maximum variation in clock period for a clock net was measured to be 660ps. Experiments were done by changing the package parasitics to measure the impact on jitter.

The large package inductance causes a high jitter in this example. Reducing the package inductance or increasing the package capacitance can lower the jitter value, according to our experiments shown below. In this case, changing the package parasitics lowered the jitter by 7% as shown in Table 1 and Figure 4

Table 1 Jitter measurements

	Total chip power	Package parasitics	Jitter
1	1.0 to 1.2W	L=583 pH, C=4pF	660.838ps
2	1.0 to 1.2W	L=541pH, C=4pF	643.873ps
3	1.0 to 1.2W	L=583pH, C=10nF	614.463ps
4	0.8 to 0.9W	L=583pH, C=4pF	466.984ps
5	1.0 to 1.2W	L= 0pH, C=4pF	160.484ps

Improving design practises, by reducing the clock network power; using gated clock design styles can also help to reduce the jitter. If portions of the clock network are turned off, the dynamic voltage drop can be less fluctuating, thus reducing the jitter.

Conclusion

In this paper, we present a comprehensive solution to clock jitter analysis. Ignoring the various complex dynamic noise sources can impact the chip yield and result in costly re-spins of SoCs. PsiWinder meets all the challenges for today's deep sub-micron designs to deliver such a solution.

References

About the Authors

Bhavana Thudi
Sr. Applications Engineer

Bhavana Thudi is an Applications Engineer at Apache Design Solutions working on power and noise analysis. Ms. Thudi received her Master of

Science degree in Electrical Engineering from University of Michigan-Ann Arbor where she worked on advanced timing analysis algorithms for switching window computation in the presence of delay noise. She holds a Bachelor of Engineering degree in Electrical Engineering from Birla Institute of Technology & Science, Pilani, India.

Ying-Shiun Li
Principal Engineer
Prior to joining Apache Design Solutions, Mr. Li worked at AmmoCore Technology, a start-up providing a scalable physical implementation solution for complex SoC designs where he focused on researching and developing clock and timing optimization algorithms to achieve timing closure of very large and complex IC designs. Mr. Li holds a Master of Science degree in electrical engineering from University Wisconsin-Madison and a Bachelor of Science degree in electrical engineering from National Taiwan University.

Ichiang Lin
Director of Timing Products
Ichiang Lin received his Ph.D. degree in computer science from University of Minnesota at Minneapolis in 1990. In 1990, he joined IBM as a technical staff in Kingston, New York. His research work created a software tool "Robin Hood" to predict and optimize CPU performance of IBM 390 mainframes. In 1993, he joined Silicon Graphics Inc MIPS division in Mountain View, California. He pioneered and developed MIPS Timing Verifier (MTV) project, a transistor-level timing analysis tool for MIPS microprocessor designs. n 1996, he founded a startup Baynacre Inc to developed a timing analysis tool AccuTime to EDA market to address the need in deep-submicron IC designs.
His company provided product sales and consulting services to microprocessor and high-end IC design projects in AMD, NEC, SGI and other companies in silicon valley. Since 2004, he joined force with Apache Design Solutions to develop a new timing solution to include the effects of power/ground noise and signal integrity. The product targets the accurate analysis on the critical path and clock tree in nano-meter IC designs.